IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Peter Burke
William Barth

Serial No. :	10/623,082	**Group Art Unit :**	2815
Filed :	July 17, 2003	**Examiner :**	Brock II, Paul E.
For :	Inter-Layer Interconnection Structure for Large Electrical Connections	**Atty Docket :**	LSI1P199 / 02-0279/1D

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Manu Kashyap

2/16/06 — Date

Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Respectfully submitted,

Timothy Croll

Reg. No. 36,771

Date: 16 FEB 06